

# **TS4984FC**

## 1.2W Stereo Audio Power Amplifier with Active Low Standby Mode

- Operating from V<sub>CC</sub> = 2.2V to 5.5V
- 1.2W output power per channel @  $V_{CC} = 5V$ , THD+N = 1%, R<sub>L</sub> = 8Ω
- 10nA standby current
- 62dB PSRR @ 217Hz with grounded inputs
- High SNR: 106dB(A) typ.
- Near-zero pop & click
- Available in a 15-bump flip-chip (lead-free)

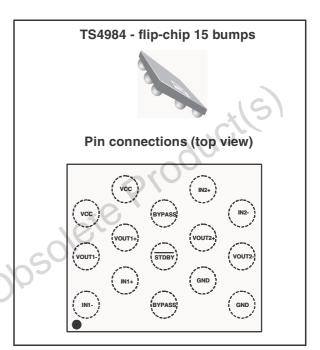
## Description

The TS4984 has been designed for top-class stereo audio applications. Thanks to its compact and power dissipation efficient flip-chip package, it suits various applications.

With a output BTL configuration, this audio power amplifier is capable of delivering 1.2W per channel of continuous RMS output power into an  $8\Omega$  load @ 5V.

An externally-controlled standby mode reduces the supply current to less than 10nA per channel. The device also features an internal thermal shutdown protection.

The gain of each channel can be configured by external gain setting resistors.



## **Applications**

- Cellular mobile phones
- Notebook & PDA computers
- LCD monitors & TVs
- Portable audio devices

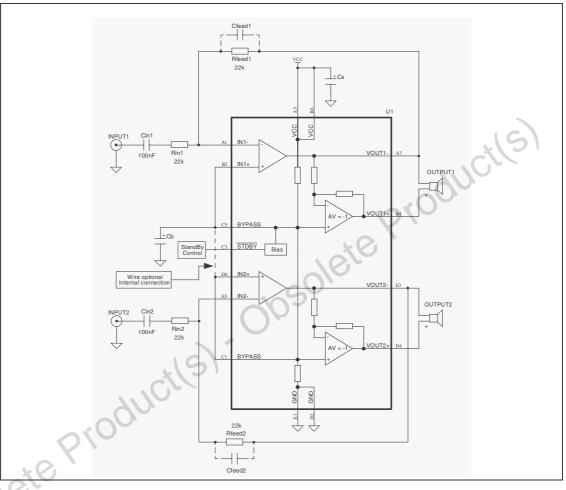
## Order Codes

Part Number	Temperature Range	Package	Packing	Marking
TS4984EIJT		Lead free flip-chip		
TS4984EIKJT	-40, +85°C	Lead free flip-chip + back coating	Tape & Reel	A84

### **Typical Application Schematic** 1

Figure 1 show a typical application schematic for the TS4984FC.

Figure 1. **Application information** 



**External component descriptions** 

	Table 1. Extern	al component descriptions
~050	Components	Functional Description
0	R <sub>in L,R</sub>	Inverting input resistors which sets the closed loop gain in conjunction with $R_{feed}$ . These resistors also form a high pass filter with $C_{in} = 1/2 \times Pi \times R_{in} \times C_{in}$ )
	C <sub>in L,R</sub>	Input coupling capacitors which blocks the DC voltage at the amplifier input terminal
	R <sub>feed L,R</sub>	Feedback resistors which sets the closed loop gain in conjunction with $\mathrm{R}_{\mathrm{in}}$
	Cs	Supply Bypass capacitor which provides power supply filtering
	Cb	Bypass pin capacitor which provides half supply filtering
	A <sub>V L, R</sub>	Closed loop gain in BTL configuration = $2 \times (R_{feed} / R_{in})$ on each channel

# 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage (1)	6	V
Vi	Input Voltage <sup>(2)</sup>	GND to V <sub>CC</sub>	V
T <sub>oper</sub>	Operating Free Air Temperature Range	-40 to + 85	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
Тj	Maximum Junction Temperature	150	°C
R <sub>thja</sub>	Thermal Resistance Junction to Ambient for Flip-chip15	180	C °C/W
P <sub>diss</sub>	Power Dissipation	Internally Limited	
ESD	Human Body Model <sup>(3)</sup>	2	kV
ESD	Machine Model	200	V
	Latch-up Immunity	200mA	

Table 2.	Key parameters and their absolute maximum ratings
Table 2.	Rey parameters and their absolute maximum ratings

1. All voltages values are measured with respect to the ground pin

2. The magnitude of input signal must never exceed V\_{CC} + 0.3V /  $G_{\rm ND}$  - 0.3V

3. All voltage values are measured from each pin with respect to supplies

	Table 5. Operating conditions				
	Symbol	Parameter	Value	Unit	
	V <sub>CC</sub>	Supply Voltage	2.2 to 5.5	V	
	VICM	Common Mode Input Voltage Range	1.2V to V <sub>CC</sub>	V	
	V <sub>STBY</sub>	Standby Voltage Input: Device ON Device OFF	$1.35 \le V_{STBY} \le V_{CC}$ GND $\le V_{STBY} \le 0.4$	V	
vs0	RL	Load Resistor	≥ 4	Ω	
$O^{\mathcal{V}}$	R <sub>OUTGND</sub>	Resistor Output to GND ( $V_{STBY} = GND$ )	≥ 1	MΩ	
	T <sub>SD</sub>	Thermal Shutdown Temperature	150	°C	
	R <sub>thja</sub>	Thermal Resistance Junction to Ambient Flip-chip15 <sup>(1)</sup>	110	°C/W	

### Table 3. Operating conditions

1. When mounted on a 4-layer PCB



#### 3 **Electrical Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I <sub>CC</sub>	Supply Current	No input signal, no load		7.4	12	mA
I <sub>STBY</sub>	Standby Current <sup>(1)</sup>	No input signal, $V_{STBY} = GND$ , $R_L = 8\Omega$		10	1000	nA
V <sub>OO</sub>	Output Offset Voltage	No input signal, $R_L = 8\Omega$		1	10	mV
Pout	Output Power	THD = 1% Max, F = 1kHz, $R_L = 8\Omega$	0.9	1.2		W
THD + N	Total Harmonic Distortion + Noise	$P_{out} = 1 Wrms, A_V = 2$ 20Hz $\leq F \leq 20 kHz, R_L = 8\Omega$		0.2	15	5%
PSRR	Power Supply Rejection	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 217Hz$	55	62		dB
ronn	Ratio <sup>(2)</sup>	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 1kHz$	55	64	dB	
Crosstalk	Channel Separation,	$R_L = 8\Omega$ , F = 1kHz		107		dB
CIUSSIAIK	Channel Separation,	$R_L = 8\Omega$ , F = 20Hz to 20kHz		82		uБ
t <sub>wu</sub>	Wake-Up Time	C <sub>b</sub> = 1µF		90	130	ms
t <sub>stby</sub>	Standby Time	$C_b = 1\mu F$		10		μs
V <sub>STBYH</sub>	Standby Voltage Level High	*(5)			1.3	V
V <sub>STBYL</sub>	Standby Voltage Level Low				0.4	V
$\Phi_{M}$	Phase Margin at Unity Gain	R <sub>L</sub> = 8Ω, C <sub>L</sub> = 500pF		65		Degrees
GM	Gain Margin	$R_{L} = 8\Omega, C_{L} = 500 pF$		15		dB
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		1.5		MHz

Table 4.  $V_{CC}$  = +5V, GND = 0V,  $T_{amb}$  = 25°C (unless otherwise specified)

1. Standby mode is activated when  $\rm V_{STBY}$  is tied to Gnd.

2. All PSRR data limits are guaranteed by production sampling tests. Dynamic measurements -  $20*\log(rms(V_{out})/rms(V_{ripple}))$ .  $V_{ripple}$  is the sinusoidal signal superimposed upon  $V_{CC}$ .



Symbol	Parameter		Min.	Тур.	Max.	Unit
I <sub>CC</sub>	Supply Current	No input signal, no load		6.6	12	mA
I <sub>STBY</sub>	Standby Current <sup>(1)</sup>	No input signal, $V_{STBY}$ = GND, $R_L$ = 8 $\Omega$		10	1000	nA
V <sub>OO</sub>	Output Offset Voltage	No input signal, $R_L = 8\Omega$		1	10	mV
Pout	Output Power	THD = 1% Max, F = 1kHz, $R_L = 8\Omega$	375	500		mW
THD + N	Total Harmonic Distortion + Noise	$P_{out} = 400 \text{mWrms}, A_V = 2$ 20Hz $\leq F \leq 20 \text{kHz}, R_L = 8\Omega$		0.1		%
PSRR	Power Supply Rejection	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 217Hz$	55	61	G	
Fonn	Ratio <sup>(2)</sup>	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 1kHz$	55	63		
Creastall	Channel Constation	$R_L = 8\Omega$ , $F = 1$ kHz		107		dB
Crosstalk	Channel Separation,	$R_L = 8\Omega$ , F = 20Hz to 20kHz	21	82		uБ
t <sub>wu</sub>	Wake-Up Time	C <sub>b</sub> = 1µF		110	140	ms
t <sub>stby</sub>	Standby Time	C <sub>b</sub> = 1μF		10		μs
V <sub>STBYH</sub>	Standby Voltage Level High	01050			1.2	V
V <sub>STBYL</sub>	Standby Voltage Level Low				0.4	V
$\Phi_{M}$	Phase Margin at Unity Gain	$R_{L} = 8\Omega, C_{L} = 500 pF$		65		Degrees
GM	Gain Margin	R <sub>L</sub> = 8Ω, C <sub>L</sub> = 500pF		15		dB
GBP	Gain Bandwidth Product	$R_{L} = 8\Omega$		1.5		MHz

Table 5.  $V_{CC}$  = +3.3V, GND = 0V,  $T_{amb}$  = 25°C (unless otherwise specified)

1. Standby mode is activated when  $V_{\mbox{\scriptsize STBY}}$  is tied to Gnd.

2. All PSRR data limits are guaranteed by production sampling tests. Dynamic measurements -  $20*\log(rms(Vout)/rms(V_{ripple}))$ .  $V_{ripple}$  is the sinusoidal signal superimposed upon  $V_{CC}$ .



able 6.	$V_{CC} = +2.6V$ , GND = 0V, $I_{amb} = 25^{\circ}C$ (unless otherwise specified)						
Symbol	Parameter		Min.	Тур.	Max.	Unit	
I <sub>CC</sub>	Supply Current	No input signal, no load		6.2	12	mA	
I <sub>STBY</sub>	Standby Current <sup>(1)</sup>	No input signal, $V_{STBY}$ = GND, $R_L$ = 8 $\Omega$		10	1000	nA	
V <sub>OO</sub>	Output Offset Voltage	No input signal, $R_L = 8\Omega$		1	10	mV	
Pout	Output Power	THD = 1% Max, F = 1kHz, $R_L = 8\Omega$	220	300		mW	
THD + N	Total Harmonic Distortion + Noise	$\begin{array}{l} P_{out} = 200 \text{mWrms},  A_V = \ 2 \\ 20 \text{Hz} \leq F \leq 20 \text{kHz},  R_L = 8 \Omega \end{array}$		0.1		%	
PSRR	Power Supply Rejection	$R_L = 8\Omega$ , $A_V = 2$ , $V_{ripple} = 200mVpp$ , Input Grounded, $F = 217Hz$	55	60		dB	
ronn	Ratio <sup>(2)</sup>	$R_L = 8\Omega, A_V = 2, V_{ripple} = 200mVpp,$ Input Grounded, F = 1kHz	55	62	CL	UB	
Creastall	Channel Constation	$R_L = 8\Omega$ , $F = 1 \text{ kHz}$		107		dB	
Crosstalk	Channel Separation,	$R_L = 8\Omega$ , F = 20Hz to 20kHz	67	82		uБ	
t <sub>wu</sub>	Wake-Up Time	$C_b = 1\mu F$		125	150	ms	
t <sub>stby</sub>	Standby Time	$C_b = 1 \mu F$		10		μs	
V <sub>STBYH</sub>	Standby Voltage Level High	01050			1.2	V	
V <sub>STBYL</sub>	Standby Voltage Level Low				0.4	V	
$\Phi_{M}$	Phase Margin at Unity Gain	$R_L = 8\Omega$ , $C_L = 500 pF$		65		Degrees	
GM	Gain Margin	$R_{L} = 8\Omega, C_{L} = 500 pF$		15		dB	
GBP	Gain Bandwidth Product	$R_L = 8\Omega$		1.5		MHz	

Table 6.	V <sub>CC</sub> = +2.6V, GND = 0V	, T <sub>amb</sub> = 25°C (unless otherwise spe	cified)		

1. Standby mode is activated when  $V_{\mbox{\scriptsize STBY}}$  is tied to Gnd.

2. All PSRR data limits are guaranteed by production sampling tests. Dynamic measurements -  $20*\log(rms(Vout)/rms(V_{ripple}))$ .  $V_{ripple}$  is the sinusoidal signal superimposed upon  $V_{CC}$ .

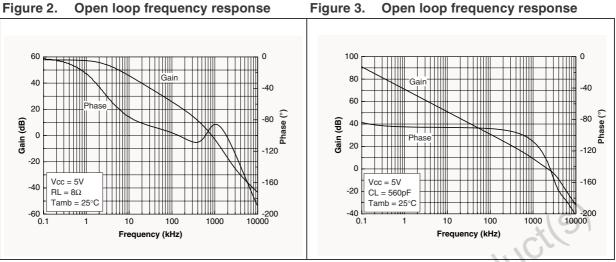


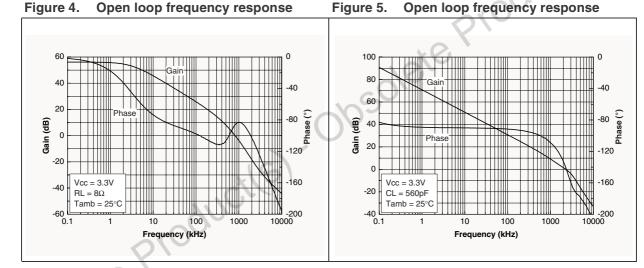
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## Table 7. Index of graphics



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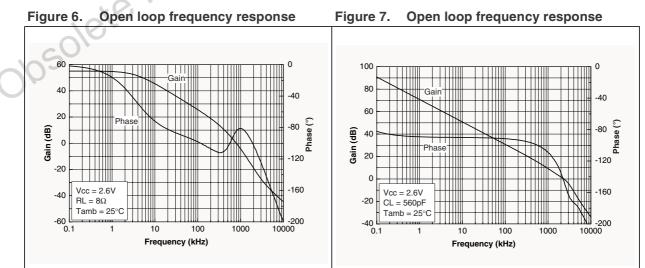


Figure 3. Open loop frequency response

-10

-20

-30

-50

-60 -70

-80

IM

100

(qB)

PSRR ( -40 Cb = 0.1µF

1000

Frequency (Hz)

 $RL >= 4\Omega$ 

UΨ

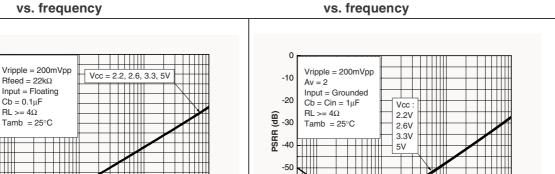
100000

Power supply rejection ratio (PSRR)

10000

#### Power supply rejection ratio (PSRR) Figure 9. Figure 8. vs. frequency

10000



-60

-70

100

1000

Frequency (Hz)

Figure 10. Power supply rejection ratio (PSRR) Figure 11. Power supply rejection ratio (PSRR) vs. frequency vs. frequency

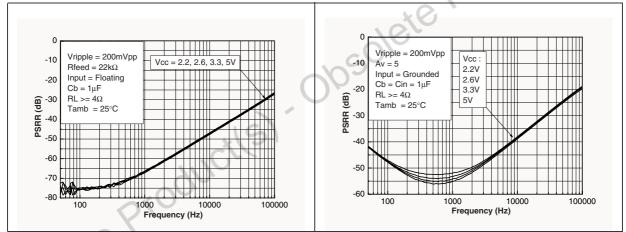
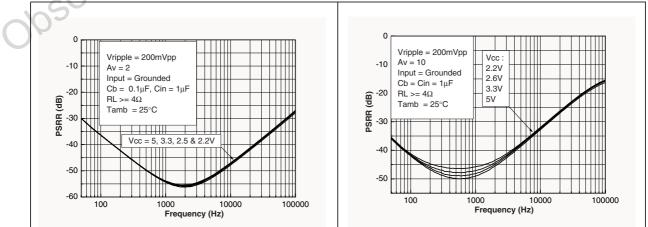


Figure 12. Power supply rejection ratio (PSRR) Figure 13. Power supply rejection ratio (PSRR) vs. frequency vs. frequency



# Figure 14. Power supply rejection ratio (PSRR) Figure 15. Power supply rejection ratio (PSRR) vs. DC output voltage vs. DC output voltage

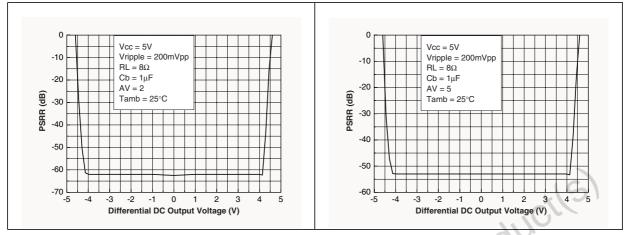


Figure 16. Power supply rejection ratio (PSRR) Figure 17. Power supply rejection ratio (PSRR) vs. DC output voltage vs. DC output voltage

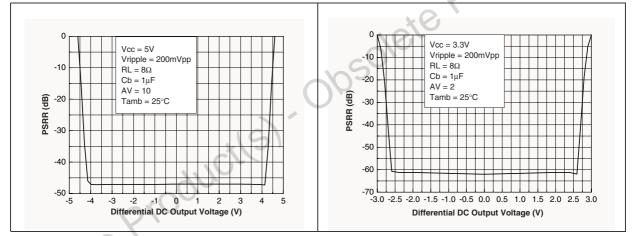
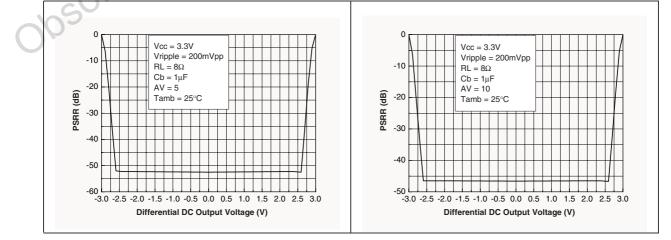


Figure 18. Power supply rejection ratio (PSRR) Figure 19. Power supply rejection ratio (PSRR) vs. DC output voltage vs. DC output voltage



# Figure 20. Power supply rejection ratio (PSRR) Figure 21. Power supply rejection ratio (PSRR) vs. DC output voltage vs. DC output voltage

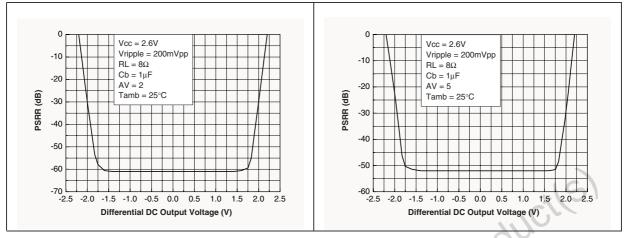


Figure 22. Power supply rejection ratio (PSRR)Figure 23.Power supply rejection ratio (PSRR)vs. DC output voltageat F = 217Hz vs. bypass capacitor

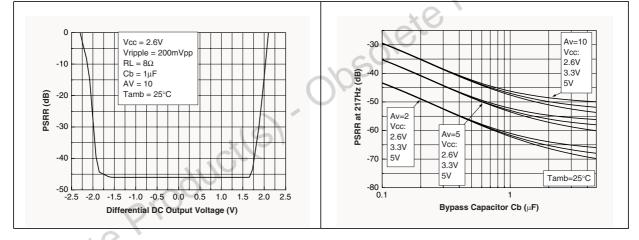
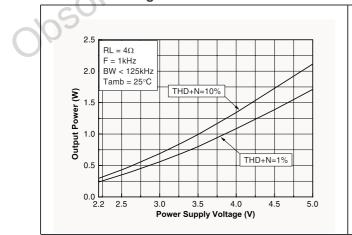
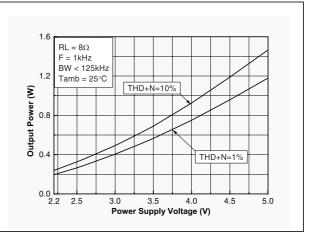


Figure 24. Output power vs. power supply voltage



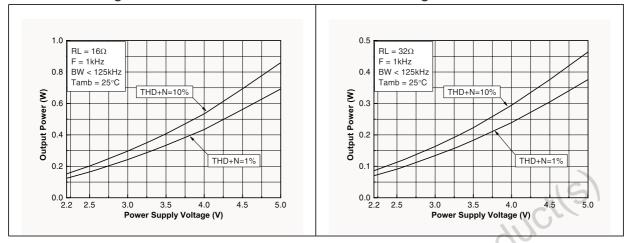
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Figure 25. Output power vs. power supply voltage



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Figure 26. Output power vs. power supply voltage





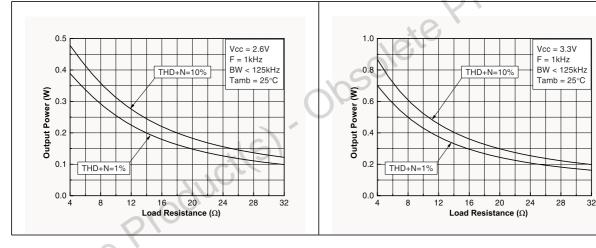


Figure 30. Output power vs. load resistor



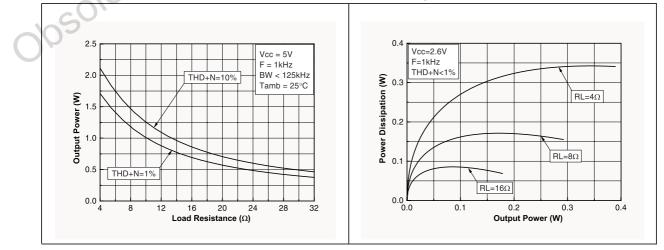


Figure 27. Output power vs. power supply voltage

Figure 29. Output power vs. load resistor



 $RL=4\Omega$ 

1.4 1.6 1.8

RL=8Ω

# per channel



1.4

1.2

1.0

0.8

0.6

0.4

0.2

0.0 L

Power Dissipation (W)

Vcc=5V

F=1kHz

THD+N<1%

0.2 0.4 0.6 0.8

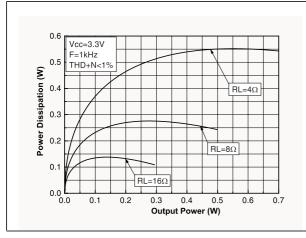
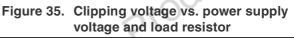


Figure 34. Clipping voltage vs. power supply voltage and load resistor



RL=16Ω

1.0 1.2

**Output Power (W)** 

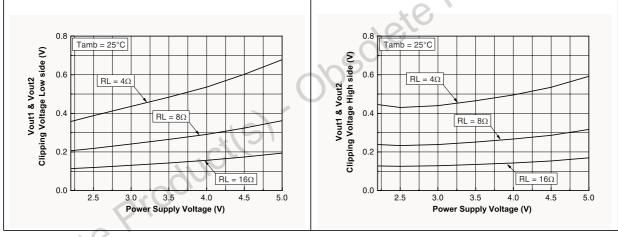


Figure 36. Current consumption vs. power supply voltage

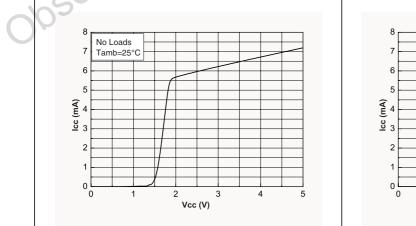


Figure 37. Current consumption vs. standby voltage at V<sub>CC</sub> = 5V

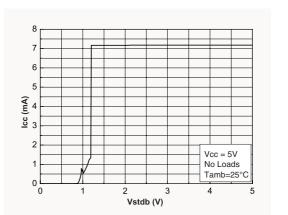
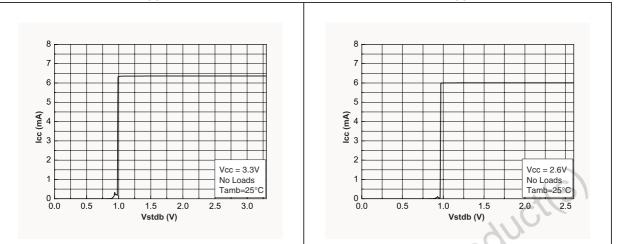
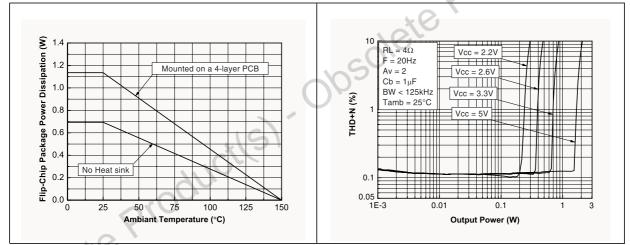
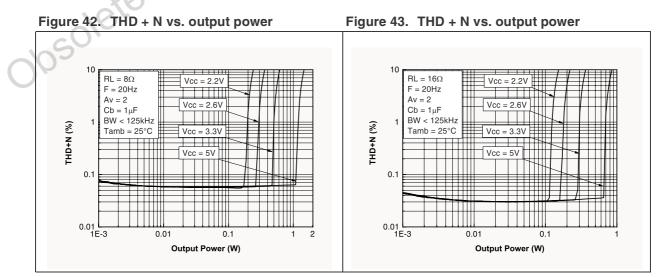


Figure 38. Current consumption vs. standby voltage at V<sub>CC</sub> = 3.3V









# Figure 39. Current consumption vs. standby voltage at V<sub>CC</sub> = 2.6V

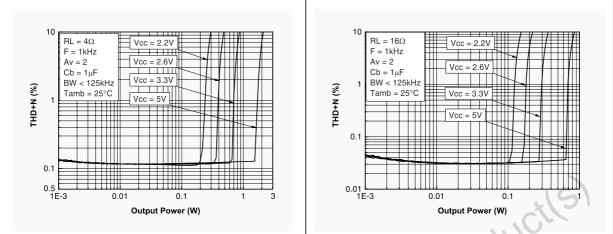
Figure 41. THD + N vs. output power

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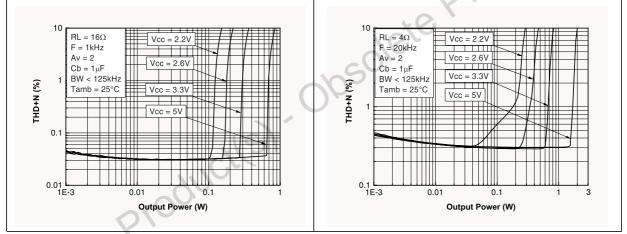
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Figure 45. THD + N vs. output power









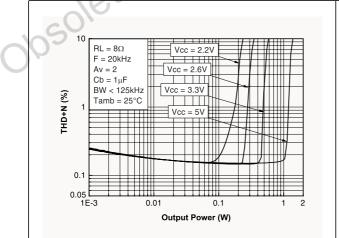
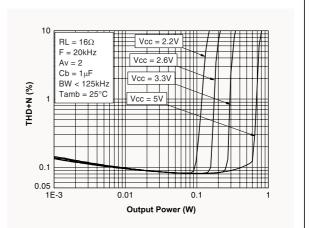




Figure 47. THD + N vs. output power



### Figure 50. THD + N vs. frequency



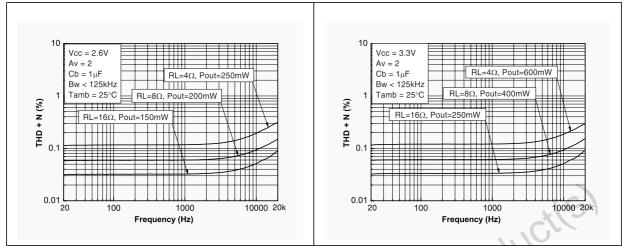
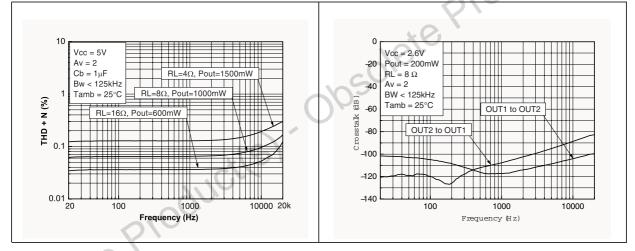
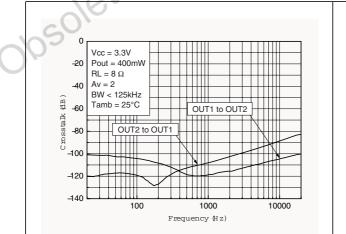




Figure 53. Crosstalk vs. frequency









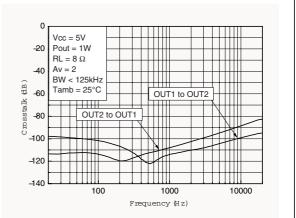


Figure 56. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

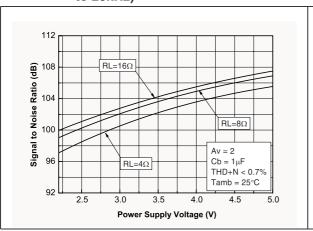
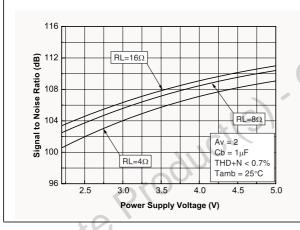
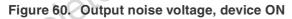
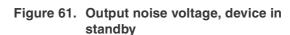


Figure 58. Signal to noise ratio vs. power supply with A weighted filter







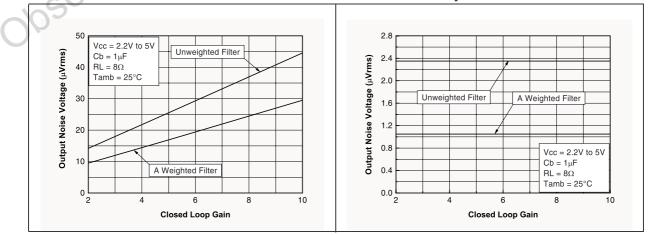


Figure 57. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

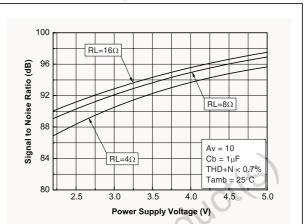
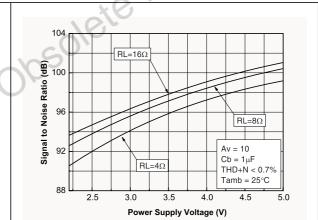


Figure 59. Signal to noise ratio vs. power supply with A weighted filter



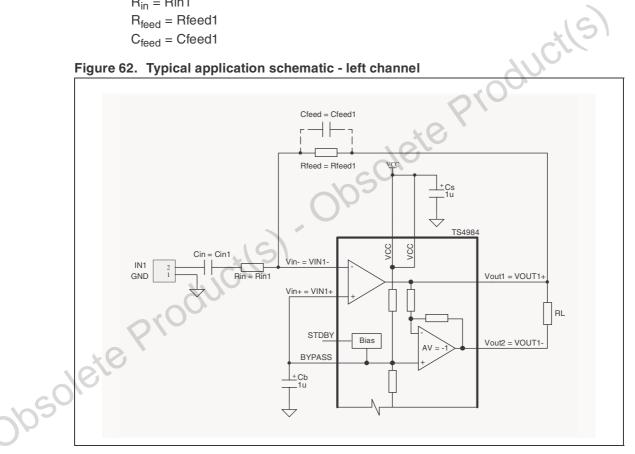
#### **Application Information** 4

The TS4984 integrates two monolithic power amplifiers with a BTL (Bridge Tied Load) output type (explained in more detail in Section 4.1). For this discussion, only the left-channel amplifier will be referred to.

Referring to the schematic in Figure 62, we assign the following variables and values:

 $V_{in} = Vin1 V_{out1} = VOUT1 +$ V<sub>out2</sub> = VOUT1- $R_{in} = Rin1$  $R_{feed} = Rfeed1$  $C_{feed} = Cfeed1$ 





#### **BTL** configuration principle 4.1

BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

> Single-ended output  $1 = V_{out1} = V_{out}$  (V), Single-ended output  $2 = V_{out2} = -V_{out}$  (V),  $V_{out1} - V_{out2} = 2V_{out}$  (V)



The output power is:

$$P_{out} = \frac{(2V_{outRMS})^2}{R_L}$$

For the same power supply voltage, the output power in a BTL configuration is four times higher than the output power in a single-ended configuration.

#### Gain in typical application schematic 4.2

The typical application schematic (Figure 62) is shown on page 18.

teproductle In the flat region (no C<sub>in</sub> effect), the output voltage of the first stage is:

$$V_{out1} = (-V_{in}) \frac{R_{feed}}{R_{in}}$$
 (V)

For the second stage:

$$V_{out2} = -V_{out1}$$
 (V)

The differential output voltage is:

$$V_{out2} - V_{out1} = 2V_{in} \frac{R_{feed}}{R_{in}}$$
 (V)

The differential gain, referred to as G<sub>v</sub> for greater convenience, is:

$$G_{v} = \frac{V_{out2} - V_{out1}}{V_{in}} = 2\frac{R_{feed}}{R_{in}}$$

 $V_{out2}$  is in phase with  $V_{in}$  and  $V_{out1}$  is phased 180° with  $V_{in}$ . This means that the positive terminal of the loudspeaker should be connected to  $V_{out2}$  and the negative to  $V_{out1}$ .

#### Low and high frequency response 4.3

In the low frequency region, Cin starts to have an effect. Cin forms with Rin a high-pass filter with a -3dB cut-off frequency:

$$F_{CL} = \frac{1}{2\pi R_{in}C_{in}} \quad (Hz)$$

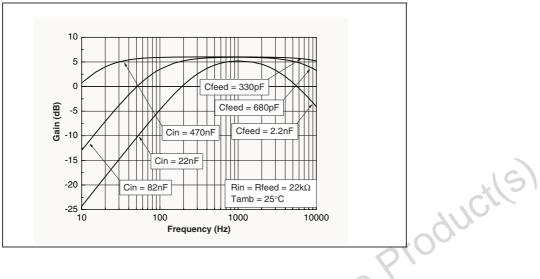
In the high frequency region, you can limit the bandwidth by adding a capacitor (C<sub>feed</sub>) in parallel with  $R_{feed}$ . It forms a low-pass filter with a -3dB cut-off frequency.  $F_{CH}$  is in Hz.

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}} \quad (Hz)$$



The following graph (*Figure 63*) shows an example of  $C_{in}$  and  $C_{feed}$  influence.





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#### Power dissipation and efficiency 4.4

Hypotheses:

- Voltage and current in the load are sinusoidal (Vout and Iout).
- Supply voltage is a pure DC source ( $V_{CC}$ ).

Productivout Regarding the load we have:

$$v_{\text{ut}} = V_{\text{PEAK}} \sin \omega t$$
 (V)

and

$$I_{out} = \frac{V_{out}}{R_L}$$
 (A)

$$P_{out} = \frac{V_{PEAK}^2}{2R_L} \qquad (W)$$

and Therefore, the average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = 2 \frac{V_{PEAK}}{\pi R_L}$$
 (A)

The power delivered by the supply voltage is:

$$\mathsf{P}_{\mathsf{supply}} = \mathsf{V}_{\mathsf{CC}} \cdot \mathsf{I}_{\mathsf{CC}_{\mathsf{AVG}}} \qquad (\mathsf{W})$$

Then, the power dissipated by each amplifier is:

$$P_{diss} = P_{supply} - P_{out}$$
 (W)

$$\mathsf{P}_{\mathsf{diss}} = \frac{2\sqrt{2}\mathsf{V}_{\mathsf{CC}}}{\pi\sqrt{\mathsf{R}_{\mathsf{L}}}} \cdot \sqrt{\mathsf{P}_{\mathsf{out}}} - \mathsf{P}_{\mathsf{out}} \qquad (\mathsf{W})$$



and the maximum value is obtained when:

$$\frac{\partial \mathsf{P}_{\mathsf{diss}}}{\partial \mathsf{P}_{\mathsf{out}}} = 0$$

and its value is:

$$\mathsf{P}_{\mathsf{dissmax}} = \frac{2\mathsf{V}_{\mathsf{cc}}^2}{\pi^2\mathsf{R}_1} \qquad (\mathsf{W})$$

Note: This maximum value is only depending on power supply voltage and load values.

The **efficiency**,  $\eta$ , is the ratio between the output power and the power supply:

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when  $V_{PEAK} = V_{CC}$ , so that:

 $\frac{\pi}{4} = 78.5\%$ 

The TS4984 has two independent power amplifiers, and each amplifier produces heat due to its power dissipation. Therefore, the maximum die temperature is the sum of the each amplifier's maximum power dissipation. It is calculated as follows:

P<sub>diss1</sub> = Power dissipation due to the 1st channel power amplifier.

P<sub>diss2</sub> = Power dissipation due to the 2nd channel power amplifier.

Total  $P_{diss} = P_{diss1} + P_{diss2}$  (W)

In most cases,  $P_{diss1} = P_{diss2}$ , giving:

Total  $P_{diss} = P_{diss1} = P_{diss2}$  (W)

or, stated differently:

Total P<sub>diss</sub> = 
$$\frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - 2P_{out}$$
 (W)

## 5 Decoupling the circuit

Two capacitors are needed to correctly bypass the TS4984. A power supply bypass capacitor  $C_S$  and a bias voltage bypass capacitor  $C_b$ .

 $C_S$  has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for  $C_S$  of 1µF, you can expect similar THD+N performances to those shown in the datasheet. For example:

- In the high frequency region, if C<sub>S</sub> is lower than 1µF, it increases THD+N and disturbances on the power supply rail are less filtered.
- On the other hand, if C<sub>S</sub> is higher than 1µF, those disturbances on the power supply rail are more filtered.

 $C_b$  has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region), in the following manner:

• If  $C_b$  is lower than 1µF, THD+N increases at lower frequencies and PSRR worsens.



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- If C<sub>b</sub> is higher than 1µF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.
- Note: The TS4984FC has two BYPASS pins. C<sub>b</sub> can be connected equally to pin C5 or to pin C1. These pins are internally connected. Connecting pin C5 and pin C1 together by an external wire is optional.

 $C_{in}$  has a non-negligible effect on PSRR at lower frequencies. The lower the value of  $C_{in}$ , the higher the PSRR.

## 4.6 Wake-up time, t<sub>wu</sub>

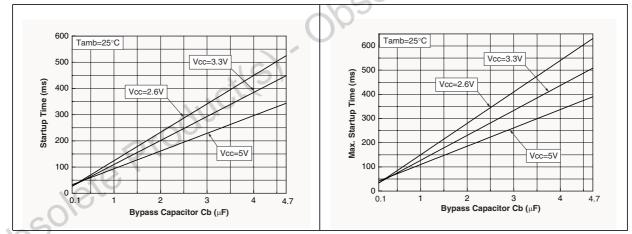
When the standby is released to put the device ON, the bypass capacitor  $C_b$  will not be charged immediately. As  $C_b$  is directly linked to the bias of the amplifier, the bias will not work properly until the  $C_b$  voltage is correct. The time required to reach this voltage is called the wake-up time or  $t_{wu}$  and specified in the tables in *Chapter 3: Electrical Characteristics* with  $C_b = 1\mu F$ .

If  $C_b$  has a value other than 1µF, please refer to the graph in *Figure 64* to establish the wake-up time value.

Due to process tolerances, the maximum value of wake-up time could be establish by the graph in *Figure 65*.



Figure 65. Maximum wake-up time vs. Cb



Note: Bypass capacitor  $C_b$  as also a tolerance of typically +/-20%. To calculate the wake-up time with this tolerance, refer to the previous graph (considering for example for  $C_b = 1\mu F$  in the range of  $0.8\mu F \le 1\mu F \le 1.2\mu F$ ).

## 4.7 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode, Bypass pin and Vin- pin are short-circuited to ground by internal switches. This allows for the quick discharge of the  $C_b$  and  $C_{in}$  capacitors.

#### 4.8 **Pop performance**

Pop performance is intimately linked with the size of the input capacitor C<sub>in</sub> and the bias voltage bypass capacitor C<sub>b</sub>.

The size of C<sub>in</sub> is dependent on the lower cut-off frequency and PSRR values requested. The size of  $C_b$  is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C<sub>b</sub> determines the speed with which the amplifier turns ON. In order to reach near zero pop and click, the equivalent input constant time,

 $\tau_{in} = (R_{in} + 2k\Omega) \times C_{in}$  (s) with  $R_{in} \ge 5k\Omega$ 

must not reach the  $\tau_{in}$  maximum value as indicated in the graph below in *Figure 66*.

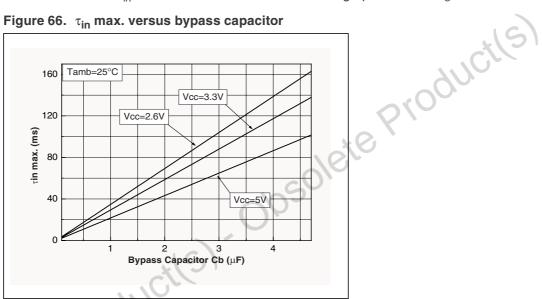


Figure 66.  $\tau_{in}$  max. versus bypass capacitor

By following the previous rules, the TS4984 can reach near zero pop and click even with high gains such as 20dB.

### **Example calculation:**

With  $R_{in} = 22k\Omega$  and a 20Hz, -3dB lower cut-off frequency,  $C_{in} = 361$ nF.

So, C<sub>in</sub> =390nF with standard value which gives a lower cut-off frequency equal to 18.5Hz.

In this case,  $(R_{in} + 2k\Omega) \times C_{in} = 9.36$ ms.

When referring to the previous graph, if  $C_b = 1\mu F$  and  $V_{CC} = 5V$ , we read 20 ms max.

This value is twice as high as our current value, thus we can state that pop and click will be reduced to its lowest value. Minimizing both C<sub>in</sub> and the gain benefits both the pop phenomena, and the cost and size of the application.



# 4.9 Application example: differential-input BTL power stereo amplifier

The schematic in *Figure 67* shows how to design the TS4984 to work in differential-input mode. For this discussion, only the left-channel amplifier will be referred to.

Let:

$$R_{1R} = R_{2L} = R_1, R_{2R} = R_{2L} = R_2$$

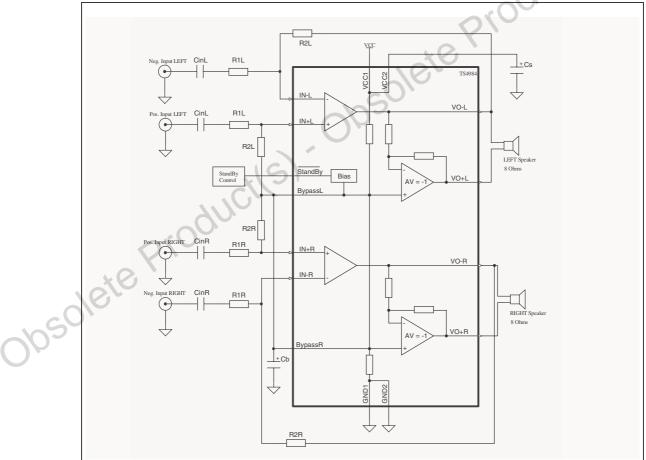
$$C_{inR} = C_{inL} = C_{in}$$

The gain of the amplifier is:

$$G_{Vdif} = 2\frac{R2}{R1}$$

In order to reach the optimal performance of the differential function,  $R_1$  and  $R_2$  should be matched at 1% maximum.

### Figure 67. Differential input amplifier configuration



The value of the input capacitor  $C_{in}$  can be calculated with the following formula, using the -3dB lower frequency required (where  ${\sf F}_{\sf L}$  is the lower frequency required):

$$C_{in} \approx \frac{1}{2\pi R_1 F_L} \quad (F)$$



Note: This formula is true only if:

$$F_{CB} = \frac{1}{2\pi(R_1 + R_2)C_b}$$
 (Hz)

is 5 times lower than  $F_L$ .

The following bill of materials is provided as an example of a differential amplifier with a gain of 2 and a -3dB lower cut-off frequency of about 80Hz.

### Table 8. Example of a bill of materials

Part Type	
20kΩ / 1%	
20kΩ / 1%	
100nF	
1µF	90
TS4984	2
	20kΩ / 1% 20kΩ / 1% 100nF 1μF

## 4.10 Demoboard

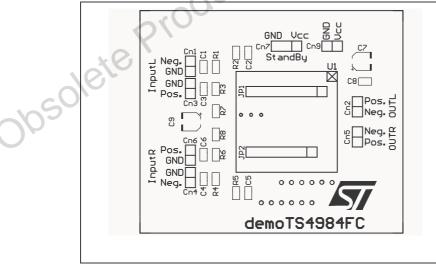
A demoboard for the TS4984 in flip-chip package is available.

For more information about this demoboard, please refer to **Application Note AN2153**, which can be found on **www.st.com**.

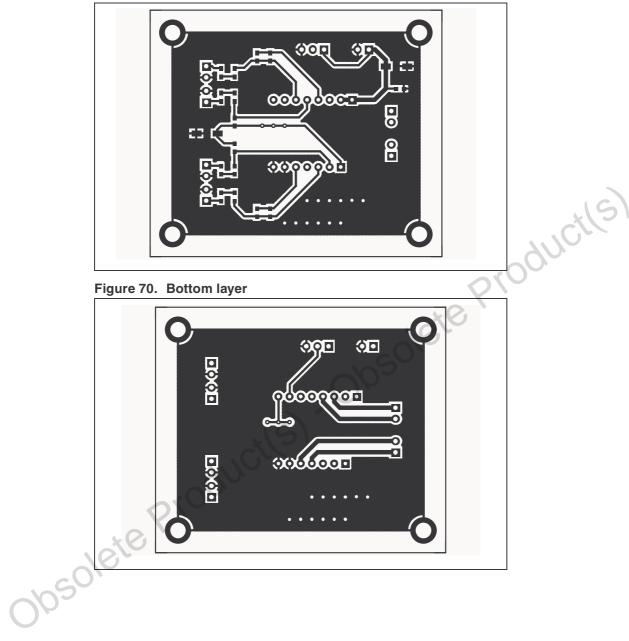
xe

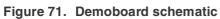
*Figure 68* shows the component locations, and *Figure 69* and *Figure 70* show top layer and bottom layers of the demoboard, respectively. *Figure 71* shows a schematic of the demoboard

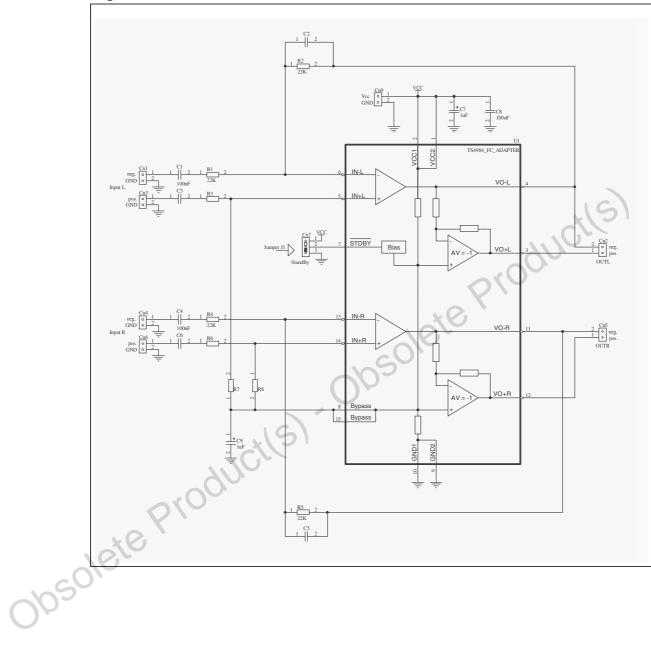
### Figure 68. Component locations











## 5 Package Mechanical Data





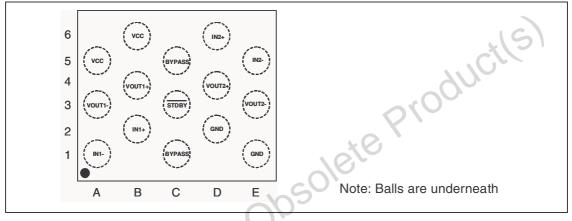


Figure 73. Marking (top view)



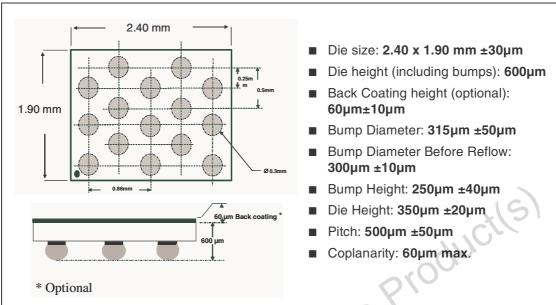
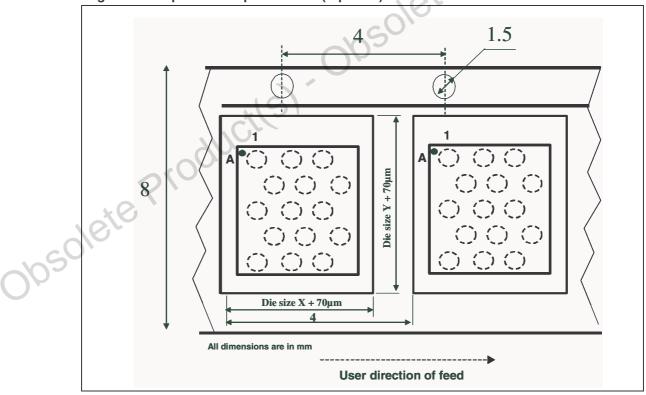


Figure 74. Package mechanical data for 15-bump flip-chip





## 6 Revision History

Date	Revision	Changes
20 May 2005	1	Initial release.
Nov. 2005	2	Typical application schematic corrected see <i>Figure 1: Application</i> <i>information on page 2.</i> Change to layout of tables in <i>Chapter 3: Electrical Characteristics on</i> <i>page 4.</i> Minor grammatical and formatting changes throughout.

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